Dr. Charvaka Duvvry

Charvaka Duvvury was a Texas Instruments fellow while he worked in the silicon technology development group. Charvaka is also a fellow of the IEEE. He is working as a technical consultant on ESD design methods and ESD qualification support. Charvaka received his PhD in engineering science from the University of Toledo. After working as a post-doctoral fellow in physics at the University of Alberta in Canada, he joined Texas Instruments, where he worked for more than 35 years. Charvaka has made numerous international presentations on ESD phenomena and protection design. He has published over 150 papers in technical journals and conferences and holds 75 patents. He has co-authored books on ESD design (ESD in Silicon Integrated Circuits, John Wiley & Sons, 2nd Edition 2002), hot carriers, and modeling of electrical overstress. He recently co-edited and authored System Level ESD Co-Design, John Wiley 2015. He is a recipient of the Outstanding Contributions award from the EOS/ESD Symposium (1990), Outstanding Mentor award twice from the SRC (1994 and 2012), and numerous best paper and best presentation awards from the EOS/ESD Symposium. He also received the IEEE Electron Devices Society Education Award (2013). He served twice as General Chair for the EOS/ESD Symposium during 1994 and in 2005. He was a contributing editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001 to 2011. Charvaka has been a member of the EOS/ESD Association board of directors since 1997, promoting university education and research in ESD. He is a co-founder and co-chair of the Industry Council on ESD Target Levels. Recently, Charvaka co-founded iT2 Technologies that features machine learning and AI-based software for ESD data analysis.